IN THE SPECIFICATION

Please replace the paragraph at page 4, lines 6-15, with the following rewritten paragraph:

In the example of Figure 46, a source terminal (S) of the P-channel transistor 11a is designated as Vdd (power supply potential) and a cathode of the EL element 15 is connected to ground potential (Vk). On the other hand, an anode is connected to a drain terminal (D) of the transistor [[11b]] 11a. Besides, a gate terminal of the P-channel transistor [[11a]] 11b is connected to a gate signal line 17a, a source terminal is connected to a source signal line 18, and a drain terminal is connected to the storage capacitance 19 and a gate terminal (G) of the P-channel transistor 11a.

Please replace the paragraph at page 7, lines 14-19, with the following rewritten paragraph:

A third invention of the present invention is a drive method of an EL display apparatus that comprises a moving-picture detection circuit which detects moving pictures and a feature extraction circuit which extracts features of video images, characterized in that the drive method of the EL display apparatus ~~implements~~ comprises:

Please replace the paragraph at page 7, lines 20-22, with the following rewritten paragraph:

a first ~~operation~~ step of changing the number of selected pixel rows depending on output data from the moving-picture detection circuit; and

Please replace the paragraph at page 7, lines 23-25, with the following rewritten paragraph:

a second ~~operation~~ step of changing the number of selected pixel rows depending on output data from the feature extraction circuit.

Please replace the paragraph at page 10, lines 4-10, with the following rewritten paragraph:

An eleventh invention of the present invention is the EL display apparatus according to the seventh invention of the present invention, characterized in that if the number of gradations is K, if channel length of the unit transistor ~~of the unit transistor~~ is L (μm), and if channel width is W (μm), a condition $(\sqrt{\ }(K/16)) \leq L/W \leq (\sqrt{\ }(K/16)) \times 20$ is satisfied.

Please delete the paragraphs at page 16, lines 4-15, in their entirety.

Please replace the paragraph at page 36, lines 15-25, with the following rewritten paragraph:

Desirably, film thickness of the thin film is such that n·d is equal to or less than main emission wavelength λ of the EL element 15 (where n is the refraction factor of the thin film[[,]] ~~or the sum of refraction factors~~ and d is the film thickness of the thin film; if two or more thin films are laminated, [[(]]n·d of each thin film is calculated[[)]] and the results are summed)[[;]] ~~d is the film thickness of the thin film, or the sum of refraction factors if two or more thin films are laminated)~~. By satisfying this condition, it is possible to more than double the efficiency of light extraction from the EL element 15 compared to when a glass

substrate is used for sealing. Also, an alloy, mixture, or laminate of aluminum and silver may be used.

Please replace the paragraph at page 37, lines 1-20, with the following rewritten paragraph:

A technique which uses a thin encapsulation film 111 for sealing instead of a sealing lid 85 as described above is called thin film encapsulation. In the case of "underside extraction (see Figure 10; light is extracted in the direction of the arrow in Figure 10)" in which light is extracted from the side of the array board 71, thin film encapsulation involves forming an EL film and then forming an aluminum electrode which will serve as a cathode on the EL film. Then, a resin layer is formed as a cushioning layer on the aluminum layer. An organic material such as acrylic or epoxy may be used for a cushioning layer. Suitable film thickness is from 1 μm to 10 μm (both inclusive). More preferably, the film thickness is from 2 μm to 6 μm (both inclusive). The encapsulation film [[74]] 111 is formed on the cushioning film layer. Without the cushioning film, structure of the EL film would be deformed by stress, resulting in streaky defects. As described above, the thin encapsulation film 111 may be made, for example, of DLC (diamond-like carbon) or an electrolytic capacitor of a laminar structure (structure consisting of thin dielectric films and aluminum films vapor-deposited alternately).

Please replace the paragraph at page 42, lines 5-16, with the following rewritten paragraph:

Preferably, the capacitor (storage capacitance) 19 should be from 0.2 pF to 2 pF both inclusive. More preferably, the capacitor (storage capacitance) 19 should be from 0.4 pF to 1.2 pF both inclusive. The capacity of the capacitor 19 is determined taking pixel size into

consideration. If the capacity needed for a single pixel is Cs (pF) and an area (rather than an aperture ratio) occupied by the pixel is Sp (square μm), a condition ~~500/S~~ 500/Sp ≤ Cs ≤ ~~20000/S~~ 2000/Sp, and more preferably a condition 1000/Sp ≤ Cs ≤ 10000/Sp should be satisfied. Since gate capacity of the transistor is small, [[Q]] Cs as referred to here is the capacity of the storage capacitance (capacitor) 19 alone.

Please replace the paragraph at page 46, lines 11-21, with the following rewritten paragraph:

Incidentally, the gate of the transistor 11a and gate of the transistor 11c are connected to the same gate signal line [[11a]] 17a. However, the gate of the transistor 11a and gate of the transistor 11c may be connected to different gate signal lines [[11]] 17 (see Figure 32). Then, one pixel will have three gate signal lines (two in the configuration in Figure 1). By controlling ON/OFF timing of the gate of the transistor 11b and ON/OFF timing of the gate of the transistor 11c separately, it is possible to further reduce variations in the current value of the EL element 15 due to variations in the transistor 11a.

Please replace the paragraph beginning at page 60, line 23 through page 61, line 7, with the following rewritten paragraph:

According to the present invention, the source driver circuit 14 is made of a semiconductor silicon chip and connected with a terminal on the source signal line 18 of the array board 71 by ~~glass-on-chip~~ chip-on-glass (COG) technology. The source driver circuit 14 can be mounted not only by the COG technology. It is also possible to mount the source driver circuit 14 by chip-on-film (COF) technology and connect it to the signal lines of the display panel. Regarding the driver IC, it may be made of three chips by constructing a power supply IC 82 separately.

Please replace the paragraph beginning at page 62, line 16, through page 63, line 2, with the following rewritten paragraph:

The same applies to cases in which the source driver circuit 14 is formed on the array board 71 by polysilicon technology such as low-temperature polysilicon technology. A plurality of inverter circuits are formed between an analog switching gate such as a transfer gate which drives the source signal line 18 and the shift register of the source driver circuit 14. The following matters (shift register output and output stages which drive signal lines (inverter circuits placed between output stages such as output gates or transfer ~~gates)~~ gates)) are common to the gate driver circuit and source driver circuit.

Please replace the paragraph beginning at page 64, line 24, through page 65, line 7, with the following rewritten paragraph:

When the display panel is used for information display apparatus such as a cell phone, it is preferable to mount (form) the source driver IC (circuit) 14 and gate driver IC (circuit) 12 on one side of the display panel as shown in Figure 9 (incidentally, a configuration in which driver ICs (circuits) are mounted (formed) on one side of a display panel is referred to as a three-side free configuration (structure). Conventionally, the gate driver IC 12 is mounted on an X side of a display area and a source driver IC 14 is mounted on a Y side). This makes it easy in the design to center the center line of a display screen 50 on the display apparatus and mount the driver ICs. Using the three-side free configuration, the gate driver circuit may be produced by high-temperature polysilicon technology, low-temperature polysilicon technology or the like (i.e., at least one of the source driver circuit 14 and gate driver circuit 12 may be formed directly on the array board 71 by polysilicon technology).

Please replace the paragraph at page 67, lines 19-25, with the following rewritten paragraph:

Incidentally, although it has been stated that the source driver IC 14 and gate driver IC 12 are made of silicon or other semiconductor wafers and mounted on the display panel, this is not restrictive. Needless to say, they may be formed directly on the display panel [[82]] 71 using low-temperature polysilicon technology or high-temperature polysilicon technology.

Please replace the paragraph at page 74, lines 3-11, with the following rewritten paragraph:

When input current is increased tenfold, output current is also increased tenfold, resulting in a tenfold increase in the EL brightness. Thus, to obtain predetermined brightness, a light emission period is reduced tenfold by reducing the conduction period of the transistor [[17d]] 11d in Figure 1 tenfold compared to a conventional conduction period. Incidentally, the tenfold increases/decreases are cited as an example to facilitate understanding and are not meant to be restrictive.

Please replace the paragraph beginning at page 75, line 23, through page 76, line 6, with the following rewritten paragraph:

In white raster display, it is assumed that average brightness over one field (frame) period of the display screen 50 is B0. This drive method performs current (voltage) programming in such a way that the brightness B1 of each pixel 16 is higher than the average brightness B0. Also, a non-display area [[53]] 52 appears during at least one field (frame) period. Thus, in the drive method according to the present invention, the average brightness over one field (frame) period is lower than B1.

Please replace the paragraph beginning at page 94, line 21, through page 95, line 7, with the following rewritten paragraph:

It is important to maintain terminal voltage of the capacitor 19 in order to reduce flickering and power consumption. This is because [[if]] any change (charge/discharge) in the terminal voltage of the capacitor 19 ~~changes (charge/discharge)~~ during one field (frame) period~~, flickering occurs when the screen brightness changes and the frame rate lowers~~ causes changes in the screen brightness, resulting in flickering at lower frame rates. The current passed through the EL element 15 by the transistor 11a must be higher than 65%. More specifically, if the initial current written into the pixel 16 and passed through the EL element 15 is taken as 100%, the current passed through the EL element 15 just before it is written into the pixel 16 in the next frame (field) must not fall below 65%.

Please replace the paragraph at page 110, lines 7-17, with the following rewritten paragraph:

The shifting interval may be varied according to locations on the screen. For example, the shifting interval may be decreased in the middle of the screen, and increased at the top and bottom of the screen. For example, a pixel row may be shifted at intervals of 200 μsec. in the middle of the screen 50, and at intervals of 100 μsec. at the top and bottom of the screen 50. This increases emission brightness in the middle of the screen 50 and decreases it around the perimeters (at the top and bottom of the screen 50)[[)]]. Needless to say, the shifting interval is varied smoothly among the top, middle, and bottom of the screen 50 to avoid brightness contours.

Please replace the paragraph beginning at page 110, line 18, through page 111, line 4, with the following rewritten paragraph:

Incidentally, the reference voltage of the source driver circuit 14 may be varied with the scanning location on the screen 50 (see Figure 146, etc.). For example, a reference current of 10 μA is used in the middle of the screen 50 and a reference current of 5 μA is used at the top of the screen 50. Varying a reference current in this way corresponding to a location in the screen 50, increases emission brightness in the middle of the screen 50 and decreases it around the perimeters (at the top and bottom of the screen 50)[[)]]. Needless to say, the reference current is varied smoothly among the top, middle, and bottom of the screen 50 to avoid brightness contours.

Please replace the paragraph at page 121, lines 3-16, with the following rewritten paragraph:

As shown in Figure 30, when the write pixel row is the (1)-th pixel row (see the 1H column in Figure [[30)]] 31), the gate signal lines 17a(1), (2), (3), (4), and (5) are selected (in the case of configuration shown in Figure 1). That is, the switching transistors 11b and the transistors 11c in the pixel rows (1), (2), (3), (4), and (5) are on. Besides, since ISEL is low, the current output circuit A which outputs 25 times larger current is selected and connected to the source signal line 18. Also, a turn-off voltage (Vgh) is applied to the gate signal line 17b. Thus, the switching transistors 11d in the pixel rows (1), (2), (3), (4), and (5) are off and current does not flow through the EL elements 15 in the corresponding pixel rows. That is, the EL elements 15 are in non-illumination mode 52.

Please replace the paragraph at page 123, lines 10-13, with the following rewritten paragraph:

Thus, each transistor 11a in the pixel row (1) deliver a current of Iw × 5 to the source signal line 18. Then, the capacitor 19 in ~~each~~ pixel row (1) is programmed with a 5 times larger current.

Please replace the paragraph at page 125, lines 1-10, with the following rewritten paragraph:

Besides, since ISEL is high, the current output circuit B which outputs 5 times larger current is selected and the current output circuit ~~1222b~~ B is connected to the source signal line 18. Also, a turn-off voltage (Vgh) is applied to the gate signal line 17b, which is in the same state as during the first 1/2 H. Thus, the switching transistors 11d in the pixel rows (2), (3), (4), (5), and (6) are off and current does not flow through the EL elements 15 in the corresponding pixel rows. That is, the EL elements 15 are in non-illumination mode 52.

Please replace the paragraph at page 129, lines 8-22, with the following rewritten paragraph:

Figure 135 shows image display status in the first field. Figure 135(a) illustrates write pixel rows (locations of odd-numbered pixel rows programmed with current ~~(voltage)~~ (voltage)). The location of the write pixel row is shifted in sequence: Figure 135(a1) → (a2) → (a3). In the first field, odd-numbered pixel rows are rewritten in sequence (image data in the even-numbered pixel rows are maintained). Figure 135(b) illustrates display status of odd-numbered pixel rows. Incidentally, Figure 135(b) illustrates only odd-numbered pixel rows. Even-numbered pixel rows are illustrated in Figure 135(c). As can be seen from Figure 135(b), the EL elements 15 of the pixels in the odd-numbered pixel rows are non-

illuminated. On the other hand, the even-numbered pixel rows are scanned in both display area 53 and non-display area 52 as shown in Figure 135(c) (N-fold pulse driving).

Please replace the paragraph beginning at page 129, line 23, through page 130, line 12, with the following rewritten paragraph:

Figure 136 shows image display status in the second field. Figure 136(a) illustrates write pixel rows (locations of odd-numbered pixel rows programmed with current ~~(voltage)~~ (voltage)). The location of the write pixel row is shifted in sequence: Figure 136(a1) → (a2) → (a3). In the second field, even-numbered pixel rows are rewritten in sequence (image data in the odd-numbered pixel rows are maintained). Figure 136(b) illustrates display status of odd-numbered pixel rows. Incidentally, Figure 136(b) illustrates only odd-numbered pixel rows. Even-numbered pixel rows are illustrated in Figure 136(c). As can be seen from Figure 136(b), the EL elements 15 of the pixels in the even-numbered pixel rows are non-illuminated. On the other hand, the odd-numbered pixel rows are scanned in both display area 53 and non-display area 52 as shown in Figure 136(c) (N-fold pulse driving).

Please replace the paragraph at page 134, lines 7-22, with the following rewritten paragraph:

The N-fold pulse driving method according to the present invention uses the same waveform for the gate signal lines 17b of different pixel rows and applies current by shifting the pixel rows at 1 H intervals. The use of such scanning makes it possible to shift illuminating pixel rows in sequence with the illumination duration of the EL elements 15 fixed to 1F/N. It is easy to shift pixel rows in this way while using the same waveform for the gate signal lines 17b of the pixel rows. It can be done by simply controlling data ST1 and ST2 applied to the shift register circuits 61a and 61b in Figure 6. For example, if Vg1 is

output to the gate signal line 17b when input ST1 is low and Vgh is output to the gate signal line 17b when input ST1 is high, ST2 applied to the shift register circuit [[17b]] 61b can be set low for a period of 1F/N and set high for the remaining period. Then, inputted ST2 can be shifted using a clock CLK2 synchronized with 1 H.

Please replace the paragraph beginning at page 134, line 23, through page 135, line 9, with the following rewritten paragraph:

Incidentally, the EL elements 15 must be turned on and off at intervals of 0.5 msec or longer. Short intervals will lead to insufficient black display due to persistence of vision, resulting in blurred images and making it look as if the resolution has lowered. This also represents a display state of a data holding display. However, increasing the on/off intervals to 100 msec will cause flickering. Thus, the on/off intervals of the EL elements must be not shorter than 0.5 [[μsec]] msec and not longer than 100 msec. More preferably, the on/off intervals should be from 2 msec to 30 msec (both inclusive). Even more preferably, the on/off intervals should be from 3 msec to 20 msec (both inclusive).

Please replace the paragraph beginning at page 135, line 17, through page 136, line 5, with the following rewritten paragraph:

Incidentally, it is preferable that the number of divisions of a black screen can be varied between still pictures and moving pictures. When N = 4, 75% is occupied by a black screen and 25% is occupied by image display. When the number of divisions is 1, a strip of black display which makes up 75% is scanned vertically. When the number of divisions is 3, three blocks are scanned, where each block consists of a black screen which makes up 25% and a display screen which makes up 25/3 percent. The number of divisions is increased for still pictures and decreased for moving pictures. The switching can be done either

automatically according to input images (detection of moving pictures) or manually by the user. Alternatively, the switching can be done according to input ~~outlet~~ content such as video on the display apparatus.

Please replace the paragraph at page 37, lines 3-12, with the following rewritten paragraph:

Needless to say, the above items also apply to the pixel configurations for current programming in Figure 38 and the like as well as to the pixel configurations for voltage programming in Figures 43, 51, 54, and the like. This can be accomplished through on/off control of the transistor 11d in Figure 38, transistor 11d in Figure 43, and transistor 11e in Figure [[51]] 115. In this way, by turning on and off the wiring which delivers current to the EL elements 15, the N-fold pulse driving according to the present invention can be implemented easily.

Please replace the paragraph at page 146, lines 3-15, with the following rewritten paragraph:

Needless to say, the drive operation in ~~(c) of Figure 33(b)~~ Figures 33(b) and 33(c) may be performed after resetting all the pixels in the screen simultaneously or during scanning. Also, it goes without saying that pixel rows may be reset (at intervals of one or more pixel rows) in interlaced driving mode (scanning at intervals of one or more pixel rows). Also, pixel rows may be reset at random. The reset driving according to the present invention involves operating pixel rows (i.e., controlling the vertical direction of the screen). However, the concept of reset driving does not limit control directions to the pixel row direction. For example, it goes without saying that reset driving may be performed in the direction of pixel columns.

Please replace the paragraph at page 147, lines 16-24, with the following rewritten paragraph:

Thus, the gate signal line 17a is controlled by the gate driver circuit 12a while the gate signal line 17c is controlled by the gate driver circuit 12b. This makes it possible to freely specify the time to turn on the transistor 11b and reset the driver transistor 11a as well as the time to turn on the transistor [[111c]] 11c and program the driver transistor 11a with current. Other parts of the configuration are the same as or similar to those described earlier, and thus description thereof will be omitted.

Please replace the paragraph at page 151, lines 11-20, with the following rewritten paragraph:

Similarly, if the shift register circuit 61a outputs a high-level signal third, a turn-on voltage is output to the gate signal lines 17c of the pixel 16(2), which now is in a state of being programmed with current (voltage). At the same time, a turn-on voltage is also output to the gate signal lines 17a of the pixel [[16(3]] 16(3), turning on the transistor 11b of the pixel 16(3) and resetting the driver transistor 11a of the pixel 16(3). Thus, the gate signal lines 17a outputs turn-on voltages for a period of 2 Hs, and the gate signal lines 17c receive a turn-on voltage for a period of 1 H.

Please replace the paragraph beginning at page 152, line 15, through page 153, line 9, with the following rewritten paragraph:

As shown in Figure 39(a), the transistors 11c and 11e are turned off and the transistor 11d is turned on. Then, the drain (D) terminal and gate (G) terminal of the current-programming transistor [[11b]] 11a are short-circuited and a current Ib flows between them

as shown in the figure. Generally, the transistor 11b has been programmed with current in the previous field (frame) and is capable of passing current (this is natural because the gate potential is held in the capacitor 19 for a period of 1F and image is displayed. However, current does not flow during a completely black display). In this state, as the transistor 11e is turned off and the transistor 11d is turned on, the drive current Ib flows through the gate (G) terminal of the transistor 11a (gate (G) terminal and the drain (D) terminal are short-circuited). Consequently, the gate (G) terminal and drain (D) terminal of the transistor 11a have the same potential, resetting the transistor 11a (to a state in which no current flows). Since the driver transistor 11b shares a common gate (G) terminal with the current-programming transistor 11a, the driver transistor 11b is also reset.

Please replace the paragraph at page 154, lines 11-25, with the following rewritten paragraph:

As in the case of Figure 33(a), if the reset mode in Figure 39(a) is synchronized with the current-programming mode in Figure 39(b), there is no problem because the period from the reset mode in Figure 39(a) to the current-programming mode in Figure 39(b) is fixed (constant). That is, preferably the period from the reset mode in Figure 33(a) or Figure 39(a) to the current-programming mode in Figure 33(b) or Figure 39(b) should be from 1 H to 10 Hs (ten horizontal scanning periods) both inclusive. More preferably, it should be from 1 H to 5 Hs or from 20 μsec to 2 msec (both inclusive). If this period is short, the driver transistors [[11]] 11a are not reset completely. If it is too long, the driver transistor 11 is turned off completely, which means that much time is required for current programming. Also, the brightness of the screen 50 is decreased.

Please replace the paragraph at page 155, lines 11-24, with the following rewritten paragraph:

If the programming current Iw is 0 A (black display), the transistor 11b is held in the state in Figure [[33(a)]] 39(a) in which it does not pass current, and thus proper black display is achieved. Also, when performing current programming for white display in Figure 39(b), the current programming is started from offset voltage of completely black display even if there are variations in the characteristics of driver transistors in pixels (the offset voltage is a starting voltage at which a current specified according to the characteristics of each driver transistor starts to flow). Thus, the time required to reach a target current value becomes uniform according to gradations. This eliminates gradation errors due to variations in the characteristics of the transistor 11a or 11b, making it possible to achieve proper image display.

Please replace the paragraph at page 162, lines 5-13, with the following rewritten paragraph:

As in the case of Figure 33(a), if the reset mode in Figure 44(a) is synchronized with the voltage-programming mode in Figure 44(b), there is no problem because the period from the reset mode in Figure 44(a) to the current-programming mode in Figure 44(b) is fixed (constant). If this period is short, the driver transistors 11 are not reset completely. If it is too long, the driver transistor 11a is turned off completely, which means that much time is required for current programming. Also, the brightness of the screen [[12]] 50 is decreased.

Please replace the paragraph at page 163, lines 19-23, with the following rewritten paragraph:

After the ~~current~~ voltage programming in Figure 44(b), the transistor 11d is turned off and the transistor 11d is turned on to deliver the programming current to the EL element 15 from the driver transistor 11a, and thereby illuminate the EL element 15, as shown in Figure 44(c).

Please replace the paragraph at page 166, lines 6-12, with the following rewritten paragraph:

Thus, in the case of a QCIF display panel, which has 220 vertical scanning lines, at least 220/5 = 44 or more lines should be grouped into a block. More preferably, 220/10 = [[11]] 22 or more lines should be grouped into a block. However, if odd-numbered rows and even-numbered rows are grouped into two different blocks, there is not much flickering even at a low frame rate, and thus the two blocks are sufficient.

Please replace the paragraph beginning at page 166, line 18 through page 167, line 2, with the following rewritten paragraph:

Incidentally, in the example in Figure 40, the gate signal lines 17b do not intersect the illumination control lines 401. Thus, there can be no defect in which a gate signal line 17b would become short-circuited with an illumination control line 401. Also, since there is no capacitive coupling between gate signal lines 17b and illumination control lines 401, ~~addition~~ capacitive load of capacitance is very small when the gate signal lines 17b are viewed from the illumination control lines 401. This makes it easy to drive the illumination control lines 401.

Please replace the paragraph at page 168, lines 19-22, with the following rewritten paragraph:

In the above example, one selection ~~pixel row~~ gate signal line is placed (formed) per pixel row. The present invention is not limited to this and a selection gate signal line may be placed (formed) for two or more pixel rows.

Please replace the paragraph at page 187, lines 10-17, with the following rewritten paragraph:

That is, when the gate driver circuit 12a outputs a turn-off voltage, the turn-off voltage is applied to the gate signal line 17a. When the gate driver circuit 12a outputs a turn-on voltage (logic low), it is ORed with the output of the OEV1 circuit by the OR circuit and the result is output to the gate signal line 17a. That is, when the OEV1 circuit is high, the turn-off voltage (Vgh) is output to the gate ~~driver~~ signal line 17a (see an exemplary timing chart in Figure 176).

Please replace the paragraph beginning at page 188, line 18 through page 189, line 2, with the following rewritten paragraph:

Incidentally, screen brightness is adjusted under the control of OEV2. There are permissible limits to changes in screen brightness. Figure 175 illustrates relationship between permissible changes (%) and screen brightness (nt). As can be seen from Figure 175, relatively dark images have small permissible changes. Thus, in performing brightness adjustments of the screen 50 under the control of OEV2 or through duty cycle control, the brightness of the screen 50 should be taken into consideration. Permissible changes should be ~~shorter~~ smaller when the screen is dark than when it is bright.

Please replace the paragraph at page 189, lines 9-18, with the following rewritten paragraph:

However, the present invention is not limited to this. The duration of the conduction period may be less than 1 H (1/2 H in Figure 143) as shown in Figure 143 or it may be equal to or ~~less~~ more than 1 H. In short, the unit length of the conduction period is not limited to 1 H and a unit length other than 1 H can be generated easily using the OEV2 circuit formed or placed in the output stage of the gate driver circuit 12b (circuit which controls the gate signal line 17b). The OEV2 circuit is similar to the OEV1 circuit described earlier, and thus description thereof will be omitted.

Please delete the paragraph at page 193, lines 7-11, in its entirety.

Please replace the paragraph at page 197, lines 3-12, with the following rewritten paragraph:

In particular, the present invention is characterized in that a first-stage current mirror circuit (current source 471) and second-stage current mirror circuits (current sources 472) are placed close to each other. If a first-stage current source 471 are connected with third-stage current sources 473 (i.e., in the case of two-stage current mirror circuit), the ~~second-stage~~ third-stage current sources 473 connected to the first-stage current source are large in number, making it impossible to place the first-stage current source 471 and third-stage current sources 473 close to each other.

Please replace the paragraph beginning at page 198, line 19, through page 199, line 2, with the following rewritten paragraph:

In the present invention, the terms "current sources 471, 472, and 473" and "current mirror circuits" are used interchangeably. That is, current sources are a basic construct of the present invention and the current sources are embodied into current mirror circuits. Thus, a current source is not limited to a current mirror circuit and may be a constant current circuit consisting of a combination of a operational amplifier 552, transistor [[471]] 471a, and register R.

Please replace the paragraph beginning at page 201, line 20 through page 202, line 3, with the following rewritten paragraph:

Incidentally, for ease of explanation, it is assumed that there are 63 current sources for a 6-bit configuration, but this is not restrictive. In the case of 8-bit configuration, 255 unit transistors 484 can be formed (placed). For a 4-bit configuration, 15 unit transistors 484 can be formed (placed). The transistors 484 constituting the unit current sources have a channel width W and channel ~~width~~ length L. The use of equal transistors makes it possible to construct output stages with small variations.

Please replace the paragraph beginning at page 205, line 16, through page 206, line 2, with the following rewritten paragraph:

Kink effect occurs when the potential of the source signal lines 18 ~~vary~~ varies due to variations in Vt of driver transistors 11a shown in Figure 1 and the like. The driver circuit 14 passes programming current through the source signal line 18 so that the programming current will flow through the driver transistor 11a of the pixel. The programming current causes changes in the gate terminal voltage of the driver transistor 11a, and consequently the

programming current flows through the driver transistor 11a. As can be seen From Figure 3, when a selected pixel 16 is in programming mode, the gate terminal voltage of the driver transistor 11a equals the potential of the source signal line 18.

Please replace the paragraph beginning at page 211, line 24, through page 212, line 11, with the following rewritten paragraph:

Incidentally, it has been described that a voltage resistance process in the range of 2.5-V to 10-V (both inclusive) is used for the source driver IC [[12]] 14. This voltage resistance is also applied to examples (e.g., a low-temperature polysilicon process) in which the source driver circuit 14 is formed directly on an array board 71. Working voltage resistance of a source driver circuit 14 formed directly on an array board 71 can be high and exceeds 15 V in some cases. In such cases, the power supply voltage used for the source driver circuit 14 may be substituted with the IC voltage resistance illustrated in Figure 121. Also, the source driver IC 14 may have the IC voltage resistance substituted with the power supply voltage used.

Please replace the paragraph at page 211, lines 12-20, with the following rewritten paragraph:

The area of a unit transistor 484 is correlated with the variations in its output current. Figure 122 is a graph obtained by varying the transistor width W of a unit transistor 484 with the area of the unit transistor 484 kept constant. In Figure [[121]] 122, the variation of the unit transistor 484 with a channel width W of 2 μm is taken as 1. The vertical axis of the graph represents a ~~relative proportion~~ variation rate, where the variation which occurs when the channel width W is 2 μm is taken as 1.

Please replace the paragraph at page 213, lines 1-5, with the following rewritten paragraph:

In Figure 122, the permissible limit to the variation rate is 3 for 64- to 256-gradation display. The variation rate varies with the ~~area~~ shape of the unit transistor 484. However, the variation rate with respect to ~~the IC voltage~~ the channel width W resistance is hardly affected by the ~~area~~ shape of the unit transistor 484.

Please replace the paragraph at page 214, lines 4-14, with the following rewritten paragraph:

Programming current Iw is output (drawn) to the source signal line via switches controlled by 6-bit image data consisting of D0, D1, D2, ..., and D5. Thus, according to activation and deactivation of the 6-bit image data consisting of D0, D1, D2, ..., and D5, currents 1 time, 2 times, 4 times, ... and/or 32 times as large as the final-stage current source 473 are added and outputted to the output line. That is, according to activation and deactivation of the 6-bit image data consisting of D0, D1, D2, ..., and D5, 0 to 63 times as large a current as the final-stage current source 473 is output from the output line (the current is drawn from the source signal line [[18]] 18).

Please replace the paragraph at page 214, lines 15-19, with the following rewritten paragraph:

Actually, as illustrated in ~~Figures 76, 77, 78, and 118~~ Figure 77, in the source driver IC 14, reference currents (IaR, IaG, and IaB) for R, G, and B, respectively, can be adjusted by registers 491 (491R, 491G, and 491B). By adjusting the reference currents Ia, the white balance can be adjusted easily.

Please replace the paragraph at page 231, lines 3-10, with the following rewritten paragraph:

The transistor groups 521b are formed, built, or placed in the left-to-right direction of the chip (in the longitudinal direction, i.e., at locations facing the output terminal 681). ~~The transistor groups 521b are formed, built, or placed in the left-to-right direction of the chip (in the longitudinal direction, i.e., at locations facing the output terminal 681).~~ According to the present invention, the number M of the transistor groups 521b is 11 (see Figure [[47)]] 47).

Please replace the paragraph at page 233, lines 1-20, with the following rewritten paragraph:

Figure 68 shows a configuration in which resistive elements 491 are formed (or placed) to control reference voltages of the three primary colors RGB independently. Of course, it goes without saying that the resistive elements 491 may be substituted with electronic regulators. Also, resistive elements 491 may be built into the source driver IC (circuit) 14. Basic current sources including ~~patent~~ parent and child current sources such as the current source 471 and current sources 472 are placed densely [[in]] with an [[a]] output current circuit 654 in an area illustrated in Figure 68. The dense placement reduces variations in outputs from the source signal lines 18. As illustrated in Figure 68, by placing them in the output current circuit [[654]] 691 at the center of the source driver IC (circuit) 14, it becomes easy to distribute current to the left and right of the source driver IC (circuit) 14 from the current source 471 and current sources 472, resulting in reduced output variations between the left and right sides (it is all right to place them in a reference current generator circuit or controller instead of the current output circuit. That is, [[654]] 691 is an area where an output circuit is not formed).

Please replace the paragraph at page 234, lines 6-9, with the following rewritten paragraph:

However, if transistors are connected in a one-to-one relationship with other transistors, any variation in the characteristics (Vt, etc.) ~~of characteristics~~ of a transistor will result in variations in the output of the corresponding transistor connected to it.

Please replace the paragraph at page 236, lines 8-12, with the following rewritten paragraph:

The use of multiple transistors for current-based delivery makes it possible to reduce variations in output current of the transistor group as a whole and further reduce variations ~~in~~ among the output current (programming current) of each terminal.

Please replace the paragraph at page 237, lines 12-22, with the following rewritten paragraph:

Now, description will be given of the relationship between the formation area of the transmission transistor group 521 and the unit transistors 484. As also illustrated in Figure [[50]] 48, a plurality of unit transistors 484 are connected per one transistor 473b. In the case of 64 gradations, 63 unit transistors 484 correspond to one transistor 473b (configuration in Figure 48). If the channel length L of the unit transistor [[473]] 484 is 10 μm and channel width W of the unit transistor 473 is 10 μm, the formation area Ts (square μm) of the unit transistor group (63 unit transistors 484, in this example) is 10 μm × 10 μm × 63 = 6300 square μm.

Please replace the paragraph at page 238, lines 11-14, with the following rewritten paragraph:

~~Also, the~~ The formation area Tmm of the transmission transistor group 521b and formation area Tms of the transmission transistor group 521c have the following relationship:

Please replace the paragraph at page 239, lines 6-20, with the following rewritten paragraph:

Incidentally, the above example is not limited to three-stage current mirror connections (multi-stage current mirror connections) shown in Figure 52. Needless to say, it is also applicable to single-stage current mirror connections. The example shown in Figure 52 involves connecting the transistor groups 521b (521b1, 521b2, 521b3, ...) each of which consists of multiple transistors 473a with the transistor groups 521c (521c1, 521c2, 521c3, ...) each of which consists of multiple transistors 473b. However, the present invention is not limited to this. It is also possible to connect a single transistor 473a with the transistor groups 521c (521c1, 521c2, 521c3, ...) each of which consists of multiple transistors 473b, or to connect the transistor groups 521b (521b1, 521b2, 521b3, ...) each of which consists of multiple transistors 473a with one transistor ~~group~~ 473b.

Please replace the paragraph at page 242, lines 17-22, with the following rewritten paragraph:

In Figure 58, the transistor group 521a and transistor groups 521b compose current mirror circuits. The transistor groups 521a ~~consists~~ consist of a plurality of transistors 472b. On the other hand, each of the transistor groups 521b consists of a plurality of transistors 473a. Similarly, each of the transistor groups 521c consists of a plurality of transistors 473c.

Please replace the paragraph at page 245, lines 2-12, with the following rewritten paragraph:

An example of the above configuration is shown in Figure 59. The transistor group 521a consists of a plurality of transistors 472b. The transistor group 521a and transistors 473a compose a current mirror circuit. The transistors 473a generates current Ic. One transistor 473a drives a plurality of transistors 473b in a transistor group 521c (the current Ic from the single transistor 473a is shunted to the plurality of transistors [[473b]] 473b). Generally, the number of transistors 473a corresponds to the number of output circuits. For example, in a QCIF+ panel, there are 176 transistors 473a in each of R, G, and B circuits.

Please replace the paragraph at page 253, lines 7-10, with the following rewritten paragraph:

As is the case with Figure 62, a plurality of transistors 473b may be provided to form a transistor group 521b1 and transistor groups 521b2. Also, a plurality of transistors 473a may be provided to form a transistor group 521a as in Figure 62.

Please replace the paragraph at page 253, lines 11-25, with the following rewritten paragraph:

Although it ~~has been stated~~ is shown in Figures 167 and 168 that the transistor 472b current is specified by the resistance R1, this is not restrictive. Electronic regulators 451a and 451b may be used as shown in Figure 170. In the configuration shown in Figure 170, the electronic regulators 451a and 451b can be operated independently. Thus, the values of the currents flowing through the transistors 472a1 and 472a2 can be changed. This makes it possible to adjust the slopes of the output currents in output stages 521c on the left and right sides of the chip. Incidentally, it is also possible to provide only one electronic regulator 451

as shown in Figure 171 and use it to control two operational amplifiers 722. The sleep switch 631 has been described with reference to Figure 63. Needless to say, a sleep switch may be placed or formed similarly as shown in Figure 172.

Please replace the paragraph at page 255, lines 4-13, with the following rewritten paragraph:

In Figure 165, the horizontal axis represents Sc × n/Sb and the vertical axis represents a fluctuation ratio. The fluctuation ratio in the ~~worst~~ best case is taken as 1. As illustrated in Figure 165, the fluctuation ratio deteriorates with increases in Sc × n/Sb. A large value of Sc × n/Sb means that the total area of the unit transistors 484 in the transistor groups 521c is larger than the total area of the transistors 473b in the transistor groups 521b when the number n of output terminals is constant. In that case, the fluctuation ratio is unfavorable.

Please replace the paragraph beginning at page 257, line 12, through page 258, line 2, with the following rewritten paragraph:

Incidentally, although it has been stated that the source driver circuits 14 are made of silicon chips, this is not restrictive. For example, a large number of source driver circuits may be formed on a glass substrate simultaneously using low-temperature polysilicon technology or the like, cut off into chips, and mounted on an array board 71. Incidentally, although it has been stated that source driver circuits are mounted on an array board 71, this is not restrictive. Any form may be adopted as long as the output terminals [[521]] 681 of the source driver circuits 14 are connected to the source signal lines 18 of the array board 71. For example, the source driver circuits 14 may be connected to the source signal lines 18 using TAB technology. By forming source driver circuits 14 on a silicon chip separately, it is

possible to reduce variations in output current and achieve proper image display as well as to reduce costs.

Please replace the paragraph at page 261, lines 1-7, with the following rewritten paragraph:

A regulator (electronic regulator) 491R for reference current adjustment is placed in a reference current circuit ~~654R~~ 691R for R, a regulator (electronic regulator) 491G for reference current adjustment is placed in a reference current circuit ~~654G~~ 691G for G, and a regulator (electronic regulator) 491B for reference current adjustment is placed in a reference current circuit ~~654B~~ 691B for B.

Please replace the paragraph at page 261, lines 15-19, with the following rewritten paragraph:

Output pads (output terminals) 681 are formed or placed on the output terminals of the IC chip and connected with the source signal lines 18 of the display panel. A bump is formed on the output pads 681 by a plating technique or ball bonding technique. The bump should be 10 to 40 μm high (both inclusive).

Please replace the paragraph beginning at page 265, line 20, through page 266, line 11, with the following rewritten paragraph:

Incidentally, it is also useful to vary the precharge voltage and gradation range among R, G, and B because emission start voltage and emission brightness of EL elements 15 vary among R, G, and B. For example, selective precharging is performed for 1/8 of all the gradations beginning with the 0th gradation (e.g., in the case of 64 gradations, image data is written after precharging for the ~~01th~~ 0th to 7th gradations) in the case of R. In the case of

other colors (G and B), selective precharging is performed for 1/16 of all the gradations beginning with the 0th gradation (e.g., in the case of 64 gradations, image data is written after precharging for the 0th to 3rd gradations). Regarding the precharge voltage, if 7 V is written into the source signal lines 18 for R, 7.5 V is written into the source signal lines 18 for the other colors (G and B). Optimum precharge voltage often varies with the production lot of the EL display panel. Thus, preferably precharge voltage can be adjustable with an external regulator. Such a regulator circuit can be implemented easily using an electronic regulator.

Please replace the paragraph at page 266, lines 12-14, with the following rewritten paragraph:

Incidentally, it is preferable that the precharge voltage is not higher than the anode voltage Vdd minus 0.5 V and ~~within~~ not lower than the anode voltage Vdd minus 2.5 V in Figure 1.

Please replace the paragraph at page 281, lines 8-13, with the following rewritten paragraph:

Also, as shown in Figure 57, a reference current INH is applied to the high-current source circuit portion. Basically, this current serves as a unit current, the required number of unit transistors 484 operate according to input data H0 to [[L5]] H5, and the total current flows in a ~~low-current~~ high-current portion as a programming current IwH.

Please replace the paragraph at page 284, line 12, through page 285, line 6, with the following rewritten paragraph:

Examples of the present invention are described by citing mainly the pixel configuration in Figure 1, but this is not restrictive. Needless to say, other pixel

configurations may also be used. Also, the configuration and layout of the gate driver circuit 12 described below are not limited to self-luminous devices such as organic EL display panels. They can also be used for liquid crystal display panels, electromagnetic induction display panels, FEDs (field emission displays), etc. For example, liquid crystal display panels may employ the configuration or arrangement of the gate driver circuit 12 according to the present invention to control a pixel's selection switching element. If two phases of the gate driver circuits 12 are used, one phase may be used to select a pixel's switching element and the other phase may be connected to one terminal of a retention capacitance in the pixel. This scheme is referred to as independent CC driving. Needless to say, the configurations described with reference to Figures 71, 73, etc. can also be used not only for the gate driver circuit 12, but also for the shift register circuits of the source driver circuit 14.

Please replace the paragraph at page 287, lines 11-17, with the following rewritten paragraph:

If P-channel transistors are used as the transistors 11 of the pixel 16, the programming current flows out from the pixel 16 to the source signal line 18. Thus, the unit ~~current circuits~~ transistors (unit current sources) 484 (see Figures 56, 57, etc.) of the source driver circuit must be N-channel transistors. In other words, the source driver circuit 14 should be configured to draw the programming current Iw.

Please replace the paragraph beginning at page 297, line 16, through page 298, line 2, with the following rewritten paragraph:

Thus, video data is proportional to programming current, which is proportional to the emission brightness of the EL element 15, which in turn is proportional to power consumption. Therefore, by performing logic processes on the video data, it is possible to

control the power consumption (power), and emission brightness[[,]] ~~and power consumption~~ of the EL display panel. That is, by performing logic processes (addition, etc.) on the video data, it is possible to determine the brightness and power consumption of the EL display panel. This makes it extremely easy to prevent peak current from exceeding a set value.

Please replace the paragraph at page 300, lines 1-13, with the following rewritten paragraph:

If the number of pixel rows is 220 and the duty ratio is 1/4, since 220/4 = 55, the brightness of the display area 53 can be varied from 1 to 55 (from brightness 1 to 55 times the brightness 1). Also, if the number of pixel rows is 220 and the duty ratio is 1/2, since 220/2 = 110, the brightness of the display area 53 can be varied from 1 to 110 (from brightness 1 to 110 times the brightness 1). Thus, the adjustable range of the ~~screen brightness~~ brightness of the screen 50 is very wide (the dynamic range of image display is wide). Also, the number of gradations which can be expressed is the same at any brightness. For example, in the case of 64 gradation display, 64 gradations can be displayed whether the brightness of the screen 50 in white raster display is 300 nt or 3 nt.

Please replace the paragraph at page 302, lines 3-12, with the following rewritten paragraph:

Figure [[174]] 175 shows a graphic plot of a detection function against changes on a screen. The horizontal axis represents screen brightness (nt) while the vertical axis represents permissible change (%). The permissible change (%) represents tolerance limits to the rate of brightness change which results when the duty ratio is changed from an arbitrary value to the next value. However, the permissible change (%) depends heavily on image content (the rate of change, scene, etc.). Also, it tends to depend on individual capability for movie detection.

Please replace the paragraph beginning at page 303, line 23, through page 304, line 17, with the following rewritten paragraph:

Thus, the drive method and display apparatus of the present invention generate at least the display mode shown in Figure 19 for display images (the display area 53 may occupy the entire screen 50 (meaning a duty ratio of 1/1 depending on the brightness of the ~~images)~~ images)) in a display panel comprising means (e.g., the capacitor 19 in Figure 1) of storing the values of current to be passed through the EL elements 15 in the pixels 16 and means (e.g., the pixel configuration in Figure 1, 43, 113, 114, 117, or the like) of turning on and off the current paths between the driver transistors 11a and light-emitting elements (e.g., the EL elements 15). Also, in duty ratio driving (a drive method or drive mode in which at least part of the screen 50 is occupied by a non-display area [[53)]] 52) at a duty ratio not higher than a predetermined value, the drive method and display apparatus of the present invention control the brightness of the screen 50 by controlling the current passed through the EL elements 15 for a unit duration of one horizontal scanning period (period of 1 H) or less. This control uses OEV2-based control (for OEV2, see Figure 175 and its description).

Please replace the paragraph beginning at page 304, line 18, through page 305, line 4, with the following rewritten paragraph:

Duty cycle control based on a unit duration of other than 1 H should be performed when the duty ratio is 1/4. Conversely, when the duty ratio is not lower than a predetermined value, duty cycle control should be performed using a unit duration of 1 H or no OEV2-based control should be performed. Duty cycle control using a unit duration of other than 1 H should be performed when a single step causes a change of 1/20 (5%) or more. More preferably, fine duty ratio ~~driving~~ control driving should be performed using OEV2-based

control even if a single change is 1/50 (2%) or less. Alternatively, it should be performed at a brightness 1/4 the maximum brightness of white raster.

Please replace the paragraph at page 309, lines 4-17, with the following rewritten paragraph:

As described earlier, programming current is proportional to video data. Thus, "the sum total of ~~programming currents~~ video data" is synonymous with "the sum total of programming currents." Incidentally, although it has been stated that the sum total of programming currents is determined over one frame (field) period, this is not restrictive. It is also possible to determine the sum total of programming currents (video data) by sampling pixels which add to programming currents at predetermined intervals or on a predetermined cycle during one frame (field) period. Alternatively, it is also possible to use the total sum before and after the frame (field) period to be controlled. Also, an estimated or predicted total sum may be used for duty cycle control.

Please replace the paragraph at page 311, lines 3-10, with the following rewritten paragraph:

As a method of controlling the brightness of the screen 50, the configuration described with reference to Figure 77 and the like is available. To vary the screen brightness 50, this method adjusts reference current, thereby varying the current flowing through the unit transistor [[634]] 484, and thereby adjusting the magnitude of the programming current. Incidentally, the method of adjusting reference current has been described with reference to Figure 53 and the like.

Please replace the paragraph beginning at page 311, line 11, through page 212, line 5, with the following rewritten paragraph:

Referring to Figure 77, reference numeral 491R denotes a regulator used to control reference current for red (R). The term "regulator" is used for ease of understanding. Actually, this component is called an electronic regulator. It is configured to adjust reference current IaR for an R circuit linearly in 64 steps in response to a 6-bit digital signal from outside. By adjusting the reference current IaR, it is possible to linearly vary the current flowing through ~~a transistor~~ transistors 472a which constitutes a current mirror with a transistor 471R. This causes changes to the current flowing through the transistors 472a in a transistor group 521a and a transistor 472b which has received a current-based delivery from the ~~transistor 472a in a transistor group 521a~~ transistors 472a. This in turn causes changes to ~~a transistor~~ transistors 473a in a transistor group 521b which constitutes a current mirror with the transistor 472b, resulting in changes to a transistor 473b which has received a current-based delivery from the ~~transistor~~ transistors 473a. Thus, since the drive current (unit current) of the unit ~~transistor~~ transistors 484 changes, the programming current can be changed. Incidentally, the same applies to reference current IaG for G and reference current IaB for B.

Please replace the paragraph beginning at page 312, line 18, through page 313, line 10, with the following rewritten paragraph:

As shown in Figure 77, an (electronic) regulator 491 is formed for each of red (R), green (G), and blue (B) circuits. Thus, by regulating the regulators 491R, 491G, and 491B, it is possible to vary (control or adjust) the current on the unit transistors 484 connected to the respective regulators. Thus, white (W) balance can be adjusted easily through adjustment of the ratio among R, G, and B. Of course, if the RGB reference currents (currents which flow

through transistors 472R, 472G, and 472B) have been adjusted at the factory, by separately installing an electronic regulator which can control the RGB electronic regulators (491R, 491G, and 491B) all at once, it is possible to adjust the white (W) balance as well. For example, in Figures ~~169 and 170~~ 170 and 171, the value of resistance R1 is adjusted so as to achieve a white balance in the RGB circuits. In this state, if switches of the electronic regulator 451 in Figures 169 and 170 are operated commonly for R, G, and B, the screen brightness can be adjusted with the white balance maintained.

Please replace the paragraph beginning at page 316, line 18, through page 317, line 2, with the following rewritten paragraph:

Figure 80 illustrates an image conversion process based on the drive method according to the present invention. The horizontal axis in Figure 80 represents gradation (number). The larger the gradation (number), the brighter the screen is. Conversely, the smaller the gradation (number), the darker the image is. The vertical axis represents frequency, i.e., the occurrence frequency[[.]] ~~The frequency represents a histogram~~ of brightness of the pixels composing an image. For example, A1 in Figure 80(a) shows that pixels with a brightness corresponding to the [[24th]] 32th gradation level occur most frequently in the image.

Please replace the paragraph at page 319, lines 11-18, with the following rewritten paragraph:

The method in Figure 80(a) can improve the brightness of the screen 50. However, the entire screen becomes whitish (poor display contrast). There are relatively small increases in current consumption (though current consumption increases in proportion to screen brightness). The method in Figure 80(b) can improve the brightness of the screen 50

and increase a display range of gradations. Consequently, there is no degradation in image quality. However, current consumption increases greatly.

Please replace the paragraph at page 321, lines 5-12, with the following rewritten paragraph:

For ease of explanation, it is assumed in the above case that the sum total of image data is determined. Calculation of the sum total of image data is often tantamount to determining the APL level of the image. Also, means of adding the sum total of image data digitally is available, and the above-mentioned ~~methods of determining the~~ sum total of image in a digital or analog fashion will be referred to as an APL level hereinafter for ease of explanation.

Please replace the paragraph at page 321, lines 13-20, with the following rewritten paragraph:

In the case of a white raster, since an image consists of 6 bits each of R, G, and B, the APL level is given by 63 × pixel count (where 63 represents the data, which corresponds to the 63rd gradation, and the pixel count of a QCIF panel is 176 × [[RGB]] 3 × 220). Thus, the APL level reaches its maximum. However, since the current consumption of the EL elements 15 vary among R, G, and B, preferably the image data should be calculated separately for R, G, and B.

Please replace the paragraph at page 322, lines 15-19, with the following rewritten paragraph:

The results produced by the multipliers 841 and 842 are added by an adder 843 and stored in a summation circuit 844. Then, the reference current control in Figure 77 and duty

cycle control in Figure 78 are performed based on the results produced by the summation circuit [[87]] 844.

Please replace the paragraph at page 330, lines 10-21, with the following rewritten paragraph:

Figure 86 shows an example of multi-point polygonal gamma curves. If image data are concentrated in high gradations, gamma curve n in Figure [[85]] 86 should be selected to increase the number of high gradations. If image data are concentrated in low gradations, gamma curve a in Figure [[85]] 86 should be selected to increase the number of low gradations. If image data are scattered, gamma curves b to n-1 in Figure [[85]] 86 should be selected. Gamma curves are selected by taking into consideration the APL level, maximum brightness (MAX), minimum brightness (MIN), and brightness distribution (SGM). Also, duty cycle control and reference current control should be taken into consideration.

Please replace the paragraph at page 333, lines 14-20, with the following rewritten paragraph:

Reference current control increases the amounts of reference current to increase screen brightness 50. Thus, large currents flow through the EL elements 15 only when the screen 50 is ~~high~~ bright. Consequently, the EL elements 15 are less prone to degradation. A problem with the reference current control is that it tends to be difficult to maintain white balance when the reference current is varied.

Please replace the paragraph at page 348, lines 9-24, with the following rewritten paragraph:

On the other hand, image data is fed into a gamma processing circuit, where gamma characteristics are determined. An APL is calculated from the image data whose gamma characteristics have been determined. A duty ratio is determined from the calculated APL. Then, a duty pattern is determined depending on whether the image is a moving picture or still picture. The duty pattern represents distribution of a non-display area 52 and display area 53. In the case of a moving picture, an undivided non-display area 52 is inserted. In the case of a still picture, a divided non-display area 52 is inserted in a scattered manner. Thus, a still picture is converted into a distribution pattern which involves inserting a divided non-display area 52 ~~and display non-display area 52~~ in a scattered manner. A moving picture is converted into a distribution pattern which involves inserting an undivided non-display area 52. The resulting distribution pattern is applied as a start pulse ST (see Figure 6) of the gate driver circuit 12b.

Please replace the paragraph at page 349, lines 1-8, with the following rewritten paragraph:

With reference to Figures 94 and 95, description has been given of how Wait time is controlled according to the duty ratio. With reference to Figures 89 to 93, description has been given of how duty cycle control is performed according to the sum of data. Figure 103 is a more detailed explanatory diagram showing how to perform duty cycle control and Wait time <u>control</u>. For ease of explanation, temporal factors and the like are expressed in a reduced form.

Please replace the paragraph beginning at page 353, line 20, through page 354, line 6, with the following rewritten paragraph:

In field-based (frame-based) duty cycle control, the numerator of the duty ratio does not need to be an integer. For example, the numerator may contain a decimal fraction as shown in Figure 107. This can be accomplished easily by controlling the OEV2 terminal. Also, the use of a duty ratio averaged over multiple frames (fields) will make ~~denominators~~ numerators contain decimal fractions. Conversely, ~~a decimal may be used as~~ the denominator of a duty ratio may contain decimal fractions. In Figure 107, the numerators are decimals such as 30.8 and 31.2. Incidentally, by using integers larger than certain values for numerators and denominators, it is possible to eliminate the need for decimal fractions.

Please replace the paragraph beginning at page 356, line 23, through page 357, line 7, with the following rewritten paragraph:

Preferably, a Wait time is provided in a change from a moving picture to a still picture as shown in Figure 111. It is recommended to determine the Wait time according to the ratio of moving pictures. "The number of different data items" on the horizontal axis in Figure [[110]] 111 indicates the ratio of moving pictures detected between a frame and the next frame. In other words, the horizontal axis represents the ratio of pixels which differ in image data between frames. Thus, the larger the value, the closer to a movie display. In Figure [[110]] 111, the closer to a movie display, the longer the Wait time.

Please replace the paragraph at page 362, lines 8-14, with the following rewritten paragraph:

In the organic EL display panel according to the present invention in Figure 147, gate driver circuits 12 are shared by the sub-screen 50b and main screen 50a. It is assumed that

the sub-screen [[50a]] 50b has 20 pixel rows or more. Thus, the screen 50 consists, for example, of 220 pixel rows of the main screen 50a and 24 pixel rows of the sub-screen 50b. Incidentally, the number of pixel rows is 176 each for R, G, and B.

Please replace the paragraph beginning at page 362, line 19, through page 363, line 4, with the following rewritten paragraph:

W/L (W is the channel width of the driver transistors and L is the channel length of the driver transistors) of the driver transistors [[17a]] 11a for the pixels in the main screen (main panel) and sub-screen (sub-panel) may be varied. Basically, W/L of the sub-screen (sub-panel) should be increased. Also, the size of pixels 16a in the main screen (main panel) 50a and the size of pixels 16b in the sub-screen (sub-panel) 50b may be varied. Also, the anode voltage Vdd or cathode voltage Vk applied to the sub-screen (sub-panel) 50b may be different from the anode or cathode ~~power supply~~ voltage of the main screen (main panel) 50a.

Please replace the paragraph at page 363, lines 5-11, with the following rewritten paragraph:

When a sub-panel [[71a]] 71b and main panel 71a are superimposed as illustrated in Figure 150(b), a cushioning sheet 1504 should be placed or formed between an encapsulation substrate 85a (encapsulation layer) and encapsulation substrate 85b (encapsulation layer). The cushioning sheet 1504 may be a plate or sheet made of metal such as a magnesium alloy or a plate or sheet made of resin such as polyester.

Please replace the paragraph at page 364, lines 13-24, with the following rewritten paragraph:

A configuration shown in Figure 154 may be used if the sub-panel 71b and main panel 71a differ in the number of source signal lines 18. Outputs of analog switches 1501a and 1501b are short-circuited and connected to the same terminal ~~1322a~~ 1522a. Also, as illustrated in Figure 155, the output of the analog switches 1501b may be connected to the voltage Vdd to prevent them from turning on. Besides, as illustrated in Figure 156, analog switches 1501a (1501a1 and 1501a2) may be placed or formed at terminations of source signal lines 18 which do not need to be connected to the sub-panel 71b. A turn-off voltage is applied to the analog switches 1501a to prevent them from turning on.

Please replace the paragraph at page 365, lines 17-25, with the following rewritten paragraph:

In addition to a push switch, the key 1572 may be a slide switch or other mechanical switch. Speech recognition may also be used for switching. For example, the switch may be configured such that display colors on the display screen 50 of the display panel will change as the user ~~speaks a phrase~~ enters a color change command by speaking such as "high-definition display," "4096-color mode," or "low-color display mode" into the phone. This can be implemented easily using existing speech recognition technology.

Please replace the paragraph at page 376, lines 13-23, with the following rewritten paragraph:

The pixel configuration in Figure 173 can perform N-fold pulse driving, duty cycle control driving, etc. if a peripheral circuit shown in Figure 174 is added. An image data signal is applied to the source signal line 18 from the video signal circuit 1732. A pixel 16

selection signal is applied to a selection signal line 2173 by an on/off control circuit 1735a, and consequently pixels 16 are selected one after another and image data is written into them. Also, an on/off signal is applied to an on/off signal line 1742 by an on/off control circuit 1735b, and consequently the ~~FED of pixels is~~ pixels of the FED are subjected to on/off control (duty cycle control).